CLAIMS

What is claimed is:

1 An input/output controller integrated circuit 1. 2 comprising: a host interface subsystem to couple to a host to 3 receive host commands and to transceive data blocks 5 6 7 8 9 with the host in response to the host commands; and a mapping controller coupled to the host interface subsystem, the mapping controller to map logical block

addresses of the host commands into physical block addresses of one or more peripherals to transceive the data blocks with the one or more peripherals.

The intedrated input/output controller of claim 1 2.

further comprising:

a peripheral interface subsystem to couple to the one or more peripherals to issue peripheral commands and to transceive data blocks with the one or more peripherals in response to the one or more peripheral commands.

- An integrated input/output (I/O) controller integrated 1
- 2 into an integrated circuit to read and write data between a host
- and one or more peripherals, the integrated I/O controller 3
- including circuits to perform:

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	receiving a high level I/O command from a host;
5	parsing the high level I/O command to determine whether
6	to read or write data;
7	the high level I/O request into one or more
8	the one or more peripheral 1,
\mathcal{M}^9	. indicating which of the one of more per-
(1)10	which respective data locations are to be accessed; and
11	high Weyel I/O request by reading of
12	writing data between the host and the one or more peripherals
13	using the respective data locations.
14	
13 14 14 11	4. The integrated 1/0 controller of claim 3, further
1 1 1 1 1 1 1 1 1 1	form.
= 3	prior to servicing the high level I/O request, storing
± ±4	data temporarily into an external cache buffer from the data
1 5	flow between the host and the one or more peripherals.
	5. The integrated I/O controller of claim 3, wherein,
1	5. The integrated I/O controller of each of the one or more peripheral I/O commands further
2	each of the one of more position indicates the number of blocks of data to be serviced.
3	indicates the number of brown
	6. The integrated I/O controller of claim 3, wherein,
1	6. The integrated 1/0 mapping the high level I/O request into one or more
2	1 I/O commands includes circuits to perior.
3	peripheral 1/0 command from an I/O request parsing a high level command from an I/O request
4	e and a ket
5	packes,

	land generating a
6	decoding the high level command and generating a
	range operation request in response thereto, and
7	generating the one or more peripheral 170
8	in response to the range operation request.
9	
	7. The integrated I/O controller of claim 3, wherein,
$\bigcap_{i=1}^{n} \lambda_{i}$	or more peripherals are score
/ A/	and each of the one or more peripheral I/O commands are Small
3/	and each of the one of more I computer System Interface (SOSI) disk I/O commands.
4	Computer System Interlace (5957)
enterio Venezio	8. The integrated I/O controller of claim 3, wherein,
: [] :	8. The integrated I/O controller of a Small
± 12	8. The integrated 1/0 ommand is a command of a Small the high level I/O dommand is a command Descriptor Block
	the high level 170 Johnna Computer System Interface (SCSI) Command Descriptor Block
4	(CDB) standard.
-i-	wherein,
± 1	9. The integrated/I/O controller of claim 3, wherein,
1 1 2	9. The integrated 1/0 controller are hard the circuits of the integrated I/O controller are hard
	wired circuits.
3	
	10. The integrated I/O controller of claim 3, wherein,
1	oircuits of the integrated I/O controller da
2	microcoded dircuits and state machines operating
3	/
4	concurrently.
	11. The integrated I/O controller of claim 3, wherein,
1	11. The integrated 1/0 conservation

2	the circuits of the integrated I/O controller are hard
3	wired circuits, microcoded circuits and state machines
4	operating concurrently.
1	12. The integrated I/O controller of claim 3, wherein,
2	the circuits of the integrated I/O controller are
3/	programmable micro-controllers operating concurrently.
1	13. An input/output controller integrated into a single
12 13	integrated circuit comprising:
÷3	a host interface subsystem to couple to a host to
74	receive host commands and to transceive data blocks
14 125 17	with the host in response to the host commands;
. 6 	a peripheral interface subsystem to couple to a
±7 ±7	peripheral to issue peripheral commands and to
8	transceive data/blocks with the peripheral in response
18 19	to the peripheral commands; and
10	a mapping controller coupled to the host interface
11	subsystem and the peripheral interface subsystem, the
12	mapping controller to map to blocks of data storage of
13	the peripheral.
1	14. The integrated input/output controller of claim 9
2	further comprising:
3	a micro-controller subsystem coupled to the host
4	interface subsystem and the peripheral interface subsystem,

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		and and
	5	the micro-controller subsystem to perform initialization and
	6	to process errors and exception events.
		15. The integrated input/output controller of claim 13
	1	1
	2 f	max coupled/to the nost installed
<u></u>	3 1	subsystem, the cache many
\}	1/5	manage entries in a cache buffer to temporarily store data of
1	6	the data flow between the peripheral and the host.
		16. The integrated input/output controller of claim 15
	<u> </u>	
	T2	gounled to the nost install
	. <u>5</u> 3 ∏ 4	interface subsystem, and
	4 ±5	subsystem, the perigneral manager to manage data storage in the manager, the buffer manager to manage data storage in the
	±2	cache buffer.
	16	17. The integrated input/output controller of claim 13
	1	17. The integrated input/output condition
	2	wherein, the host interface subsystem includes a fibre channel
	3	the host interface subsystem host port to transceive data with the host using a fibre
	4	
	5	channel protocol.
		18. The integrated input/output controller of claim 13
	1	
	2	wherein, the host interface subsystem includes
	;	3 the host interface such
ı		

		a host exchange controller to control the physical
	4	a host exchange controlled
	5	connection and protocol of the host.
	3	
	1	19. The integrated input/output controller of claim 13
	2 wh	erein,
	Ā	host interface subsystem includes
X	∀ ९	a command decode controller to decode host
1	V 4	/
	5	Commands.
		/ controller of claim 13
	:=1	20. The integrated input output controller of claim 13
	`2 W 	interface subsystem includes
	1 2 2 3 4 5	exchange controller to controller
	4	physical connection and protocol of the peripheral.
	¹ 5	physical connection and process
	l efe	/ at at claim 13
	di.	21. The integrated input/output controller of claim 13
	1 2	
	2	wherein, the peripheral interface subsystem includes a
	3	the peripheral
	4	the peripheral interface of the peripheral Fibrechannel disk port to transceive data with the peripheral
	5	using a Fibrechannel protocol.
	3	•
		22. A method of processing host write commands between a
	1	host and one or more peripherals, the method comprising:
	2	host and one or more peripheral, the
	2	receiving a high level write command from a host, the
	3	receiving a fight for the high level write command requesting to write data from the
	4	host transparently to one or more peripherals;
	5	host transparence, co -
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	mapping the high level write command into one or more
6	mapping the high level
7	low level peripheral write commands, the one or more low
8	low level peripheral write commands indicating data storage level peripheral write commands indicating data storage
9	level peripheral witte data from locations in the one or more peripherals into which data from
	the host is to be written;
10	servicing the high level write command by receiving data
11	from the host for storage into the data storage locations in
12	from the host for storage into the
13	the one or more peripherals; and
	writing the data from the host into the data storage
14	locations in the one or more peripherals in response to the
15	one or more low level peripheral write commands.
16	one or more low level portage
Ti L	. od further comprising:
16 1 1 1 1 1	23. The method of claim 22 further comprising:
	prior to writing the data from the host into the data
2 3 4 4	prior to writing the data from the host storage locations, temporarily storing the data from the host
# 14	into a buffer memory.
4	
a.Ē	24. The method of claim 22 wherein,
1	24. The method of critical and the number of the high level write command indicates the number of
2	blocks of data to be written from the host.
3	blocks of data to be willton
	/ road commands between a host
1	25. A method of processing host read commands between a host
2	and one or more peripherals, the method comprising:
	high level read command from a nost, the
3	high level read command requesting to transparently read data
4	from the one or more peripherals to the host;
5	from the one or more periphoral
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	road command into one or more low
6	mapping the high level read command into one or more low
7	level peripheral read commands, the one or more low level
8	l commands indicating data storage -
9	the one or more peripherals from which data is to be accessed
	read out to the host;
10	servicing the high level read request by reading data
11	from the data storage locations in the one or more
12	from the data storage local to one or more low level
13	peripherals in response to the one or more low level
14	peripheral read commands; and
15	providing the data to the host.
	26. The method of claim 25 further comprising:
al O	the providing the data to the host, temporary
12	storing the data from the one or more peripherals into a
_3	
4	buffer memory.
	27. The method of claim 25 wherein,
31	27. The method of Claim 27 the high level read command indicates the number of
2	the high level read common the host.
3	blocks of data to be read into the host.
	controller comprising:
1	28. An integrated input/output controller comprising:
C) 2h	onductor integrated Circuit indians
50°	a semiconductor a host interface to couple to one or more
	servers to transceive data between the one or more
7	servers to transcerve
5	response to host commands,
6	

	a mapping controller coupled to the host	
7	interface subsystem, the mapping controller to map to	
8	blocks of data storage of a peripheral, and	
9	a micro-controller coupled to the host interface	
$10 \bigwedge$	a micro-controller coaffer to perform	
11	subsystem, the micro-controller to perform initialization and handle error and exception handling	g
12	initialization and nandle ellor	
13	events.	
	/ throller of claim 28	
1 29. T	he integrated input/output controller of claim 28	
	/ land fibre channel	
1 13	the host interface subsystem includes a fibre channel	
wherein, host p state of the	oort to transceive data with the one or more servers	
using	a fibre channel protocol.	
i i	The integrated input/output controller of claim 28	
±2 wherein,		
2 WHELEIM	the host interface subsystem includes a command decode	,
antr	coller to receive and decode host command packets.	
4 CONCI	/	
21	The integrated input/output controller of claim 30	
1 31.		
2 wherein,	the command decode controller to further validate a h	ost
3	the command decode or mand and to initiate execution of the host command by t	.he
4 comm	egrated input/output controller.	
5 inte	egrated input/output	
	The integrated input/output controller of claim 30	
1 32.	The integrated inposition	
2 wherein,	WEA	/sm
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3	the command decode controller to \int further validate a host
4	command and to queue the host command in a queue to be
5	executed in an order, the command queue associated with a
6	volume accessible by one of the one or more a servers.
ĭ	
1	33. The integrated input/output controller of claim 30
2	wherein,
3	the command decode controller to further validate a host
4	command and to determine that the host command is invalid,
 5	the host command is passed to the micro-controller subsystem
6	to process the invalidity.
i ale	
1 1 2	34. The integrated input/output controller of claim 30
2	wherein,
±3	the host command packets are high level input/output
4	requests.
4	
1	35. The integrated input/output controller of claim 28
2	further comprising:
3	a peripheral interface to couple to one or more
4	peripheral devices and transceive data between the one or
5	more peripheral devices and the one or more servers coupled
6	to the host port.
1	36. The integrated input/output controller of claim 28
2	wherein,

	the integrated input/output controller is an integrate	d
3	RAID controller to transceive data between one or more disk	.S
4	RAID controller to transceive data for integrated input/output	
5	of at least one disk array and the integrated input/output	
6	controller further comprises:	
7	a disk interface to douple to the one or more	ne
80/	disks of the at least one disk array to transceive the	
	data to or from the one or more servers; and	ler
10	the mapping controller is a RAID mapping control	.102
	to flexibly control the mapping of blocks of data	
11	storage on the one one of more disks of the at least one	
12	disk array.	
43 -		
## ###	37. The integrated Input/output controller of claim 36	
. <u>1</u>		
13 1 1 2 w	the one or more disks of the at least one array of o	lisks
= 3	are magnetic storage media, optical storage media or	
4		
1 5	semiconductor storage media.	
	38. The integrated input/output controller of claim 36	
1	38. The integrated input/output	
2	the disk interface subsystem includes one or more f	ibre
3	the disk interface subsystem and the disk interface subsystem and the channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel disk ports to transceive data with the one or more channel data with the one or more channel data with the one or more channel data with the order of the channel data with the channel data with the order of the channel data with the order of the channel data with the channel data with the channel data with the channel data with the order of the channel data with the ch	ore
4	channel disk ports to transceive data sing a fibre channel	nel
5	disks of the at least one disk array using a fibre channel	
6	protocol.	
	lar of claim 28	3
1	$\frac{1}{39}$. The integrated input/output controller of claim 28	
2	wherein,/	
_	<i>,</i>	EA/sm

		mapping automation.	•
	3	the mapping controller provides RAID mapping automation.	
	3		
	1	40. The integrated input/output controller of claim 28	
	2 when	the mapping controller is programmable hardware to	
	3	the mapping controller is progration the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexibly control the mapping of blocks of data storage on the flexible control the mapping of blocks of data storage on the flexible control the mapping of blocks of data storage on the flexible control the mapping of blocks of data storage.	ıe
	4	flexibly control the mapping of blocks array.	
٠, ٨	5	one or more disks of the at least one disk array.	
W W		integrated input/output controller of claim 28	
	1		
	2 wh	the mapping controller to receive a requested command	
	<u>.</u> 3	input packet to generate expanded command output packets in	n
	<u>-</u> 4	input packet to generate expands	
	<u></u>	response thereto, the requested command input packet	
	2 wh	functions as a logical address and the expanded command	
	<u>-</u> 7	output packets function as physical addresses.	
		/ controller of claim 28	
	4 1	42. The integrated input/output controller of claim 28	
		further comprising:	lager
			cache
	3	I ample to a Cache 201	
	4	himaly to flexibly or	
	5	data to and from the mapped as	110
	6	one or more disks of the at least one disk array.	
	7	1	
		43. A storage area network for central data storage and	£
1	1	management the storage area network comprising:	
	2	management the storage arca management to some server to couple to a network;	
	3	at least one server to the w	EA/sm
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at least one disk array having a plurality of disks; and 4 at least one fibre channel controller t/b couple to at 5 least one server and at least one disk array, the at least 6 7 one fibre channel controller to read and write data between 8 the at least one server and the at least one disk array, the at least one fiber channel controller /having a cache memory, 11 a microprocessor to initialize the fiber channel 12 controller upon power up and reset, a programmable random acces/s memory (PRAM) to store 13 1<u>4</u> initialization instructions in /firmware, and 15 16 17 a hardware redundant array of independent disks (RAID) controller to control the reading and writing of data between the at least one server and the at least one disk array. nî. The storage area network of claim 43 for central data 44. storage and management, whetein the hardware RAID controller 3 includes, 4 a host interface to couple to the at least one 5 server to receive data from the at least one server for 6 storage into the one or more disks of the at least one 7 disk array and to transmit data to the at least one 8 server $f \not b r$ data accessed from the one or more disks of 9 the at fleast one disk array; 10 a disk interface to couple to the one or more 11 disks of the at least one disk array to transmit data 12 to the one or more disks of the at least one disk array

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13	for storage and to receive data from the one or more
14	disks of the at least one disk array when accessed,
15	a RAID mapping controller to flexibly control the
16	mapping of blocks of storage on the one or more disks
17	of the at least one disk array, and
18	a micro-controller coupled to the host interface
19	subsystem, the disk interface subsystem, and the RAID
20	mapping subsystem, the microfcontroller to handle non-
21	data flow commands, error and exception handling events
22	as well as system initialization.
'L	
22 1 1 1 2 7 3	44. The storage area network of claim 43 for central data
_2	storage and management, wherein,
3	the cache memory to provide a cache data buffer and a
<u></u> 4	cache table buffer for the integrated RAID controller
±5	integrated circuit.
*5	
1	46. The storage area hetwork of claim 43 for central data
2	storage and management, wherein,
3	the plurality ϕ f disks of the at least one array of
4	disks are magnetic storage media, optical storage media or
5	semiconductor storage media.
1	47. An integrated input/output (I/O) controller comprising:
2	a semiconductor integrated circuit including,
3	a host command manager to manage high level host
4	I/O requests from a plurality of hosts;
	1

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a mapping engine to map high level host I/O
a mapping engine state and
requests into low level \(\frac{1}{0}\) commands; and a low level command manager to manage data read
7 a low level command manager, to an aperipheral
accesses into alla out
dovice in response to the low level 1/0 commen
$\frac{1}{48.}$ The integrated input/output (I/O) controller of claim 47
2 further comprising:
manager to arbitiate door,
more servers and to control data reads and data man
into and out of a buffer memory.
5
49. The integrated input output (I/O) controller of claim 47
1 49. The integrated inputy
into and out of a buffer memory. 49. The integrated input output (I/O) controller of claim 47 further comprising: a micro-controller to handle non-data flow commands, system initialization and error handling exception conditions.
a micro-controller to handling
a micro-control a micro-control commands, system initialization and error handling
exception conditions.
1 50. The integrated input/output (I/O) controller of claim 47
2 wherein the integrated I/O controller is a RAID controller
the integrated 1/3 and the peripheral device is a plurality of disks
and the peripheral device 13 1
responsive to disk I/O commands.
1 51. A method of transceiving data to a plurality of disks in
comprising:
2 an integraced circum,
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3	receiving an I/O request from at least one server, the
4	I/O request indicating a volume to access;
5	mapping the I/O request into a disk I/O command, the
6	disk I/O command indicating one or more disks of the

plurality of disks to process/the disk I/O command; and managing a data read or a data write access to the plurality of disks in response to the disk I/O command.

The method of clayin 51 for transceiving data to a 52. plurality of disks in an integrated circuit further comprising:

arbitrating a data read or a data write access to a buffer memory to *temporarily store the data prior to the data read or data write access to the plurality of disks.

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